AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-24. (Cancelled)

25. (Withdrawn) A hierarchal memory structure, comprising:

at least one redundant predecoder adapted to be shifted in, for at least one active predecoder of a plurality of active predecoders adapted to be shifted out.

26. (Withdrawn) The structure of Claim 25 further comprising at least one higher address predecoded line coupled to at least said redundant predecoder.

27. (Withdrawn) The structure of Claim 25, further comprising at least one lower address predecoded line coupled to at least one of said plurality of active predecoders and paired with [said] at least one higher address predecoded line.

28. (Withdrawn) The structure of Claim 25, further comprising at least one shift pointer adapted to shift in said redundant predecoder.

29. (Withdrawn) The structure of Claim 25, further comprising shift circuitry adapted to at least shift in said at least one redundant predecoder.

30. (Withdrawn) The structure of Claim 29, wherein at least one of said active predecoders is adapted to fire for current address mapping.

31. (Withdrawn) The structure of Claim 29, wherein said redundant predecoder is adapted to fire for previous address mapping.

32. (Withdrawn) The structure of Claim 29, further comprising a shift line coupled to at least said shift circuitry.

33. (Withdrawn) The structure of Claim 29, further comprising an addrcurrent line coupled to at least one of said plurality of active predecoders.

34. (Withdrawn) The structure of Claim 29, further comprising an addrprev line coupled to at least said redundant predecoder.

35. (Withdrawn) A hierarchical memory structure comprising:

a synchronously controlled global element;

a self-timed local element interfacing with said synchronously controlled global element;

a plurality of predecoders, wherein at least one of said plurality of predecoders is adapted to fire for current predecoding; and

at least one predecoder being adapted to fire for previous predecoding.

36. (Withdrawn) The memory structure of Claim 35, further comprising a redundant block communicating with at least one predecoder.

37. (Withdrawn) The memory structure of Claim 35, wherein said global element includes a global predecoder.

38. (Withdrawn) The memory structure of Claim 35, wherein said global element comprises at least one global decoder.

39. (Withdrawn) The memory structure of Claim 35, wherein said global element comprises at least one global sense amplifier.

40. (Withdrawn) The memory structure of Claim 35, wherein said local element comprises a plurality of memory cells forming at least one cell array.

41. (Withdrawn) The memory structure of Claim 35, wherein said local element comprises at least one local sense amplifier.

42. (Withdrawn) The memory structure of Claim 35, further comprising at least one predecoder line communicating with at least one of said plurality of predecoders adapted to fire for current predecoding.

43. (Withdrawn) The memory structure of Claim 35, further comprising at least one predecoder line communicating with said predecoder adapted to fire for previous predecoding.

44. (Previously Presented) A method of providing redundancy in a memory structure, comprising:

shifting out a at least one first predecoder of a pluarality of first predecoders; and

shifting in a second predecoder.

45. (Previously Presented) The method of claim 44, comprising shifting predecoded lines coupled to at least one of said first and second predecoders.

46. (Previously Presented) The method of claim 44, comprising using shifting circuitry coupled to at least one of said first and second predecoders.

47. (Previously Presented) The method of Claim 44 comprising at least one higher address predecoded line coupled to at least said second predecoder.

48. (Previously Presented) The method of Claim 47 comprising at least one lower address predecoded line coupled to at least said active predecoder and paired with at least one higher address predecoded line.

49. (Previously Presented) A method of providing redundancy in a hierarchical memory structure, comprising:

identifying at least one first predecoder of a plurality of first predecoders;

shifting out said identified at least one first predecoder; and

shifting in at least one second predecoder.

50. (Previously Presented) The method of Claim 49 comprising shifting predecoded lines coupled to at least one of said first and second predecoders.

51. (Previously Presented) The method of claim 49 comprising using shifting circuitry coupled to at least one of said first and second predecoders.

52. (Previously Presented) The method of Claim 49 comprising at least one higher address predecoded line coupled to at least one of said first and second predecoders.

53. (Previously Presented) The method of Claim 53 comprising at least one lower address predecoded line coupled to at least one of said first and second predecoders and paired with said at least one higher address predecoded line.

54. (Previously Presented) The method of Claim 49 comprising at least one of said first predecoders adapted to fire for current address mapping.

55. (Previously Presented) The method of Claim 49 comprising said at least one second predecoder adapted to fire for previous address mapping.

56. (Previously Presented) The method of Claim 49 comprising shifting in said second predecoder using shift circuitry.